ABSTRACT OF THE DISCLOSURE

A processor having a floating point execution unit with improved parallelism in the adder (add/subtract) unit is disclosed. A preferred aspect of the invention is a new use of the compare logic in the floating point execution unit, coupled with an end-around-carry bit value calculator, to allow the correct rounding choice of the operands to be made before the mantissa portions of the operands are subtracted (added) rather than after.

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